to accomplish the impossible but to achieve a transmission line topology in which the reflections are small enough to not degrade the load's valid detection of logic-1 and logic-0 states.

Parallel termination resistors should always be placed as close to the end of a transmission line as possible to minimize stub lengths between the terminator and the IC pin. Stubs appear as transmission lines of their own and can cause more reflections if not kept short. It can be difficult to squeeze termination components close to IC pins, but efforts should be made to achieve the best practical results.

Terminating a line at one end as shown in Fig. 18.6 is proper for a unidirectional signal, because the driver launches a signal into one end of the transmission line, and the termination is placed at the load end to prevent reflections. When both ends of the line are driven, as is the case with bidirectional buses, both ends require termination. The resistor at the driver end appears as a normal DC load, and the resistor at the far end serves as a terminator.

Situations commonly arise in which a bus has more than one load. A microprocessor bus must typically connect to several memory and peripheral ICs. The transmission line topology must be laid out carefully to minimize the potential for harmful reflections. The best scenario is to create a single, continuous transmission line terminated at each end that snakes through the circuit board and contacts each IC so that the stubs to each IC are of negligible length as shown in Fig. 18.7. When an IC at either end drives the bus, it drives a single transmission line that is terminated at the other end. When an IC in the middle drives the bus, it drives two equivalent transmission lines that are terminated at their ends. Graphically, the single transmission line can be drawn as shown using multiple segments connected by nodes that indicate tap points for individual ICs. Because nodes are drawn with the assumption of negligible length and constant voltage, they are conceptually transparent to the transmission line segments on each side. Keep in mind that not all buses require a perfect transmission line topology. Depending on their wire lengths and the switching times of the drivers, the wires may be regarded as idealized and not require special handling.

Many nonideal topologies exist in which no attempt has been made to shorten stubs and there is really no identifiable transmission line "backbone." Instead, the wiring is fairly random. A topology like this works either by virtue of the fact that the signal transition times are slow enough to not

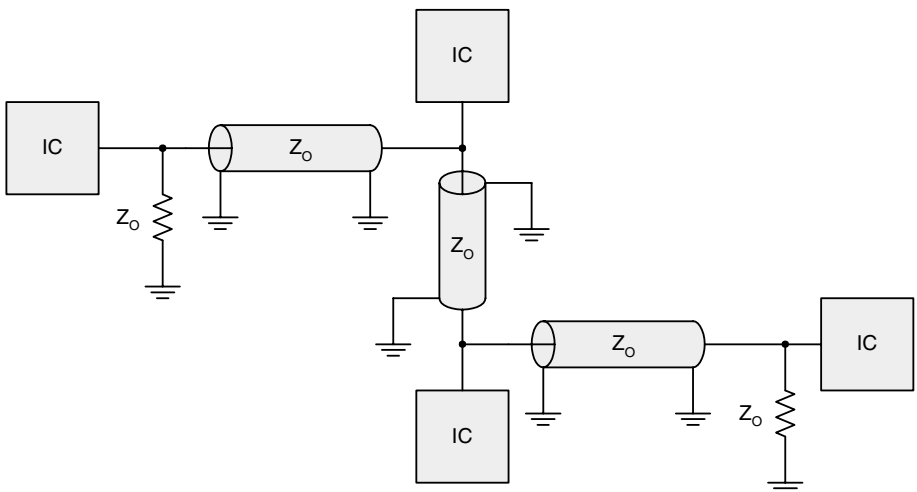

FIGURE 18.7 Multidrop transmission line topology.

make transmission line effects significant, or by plain luck. If the former, the circuit is perfectly valid, because there is no reason to cause wiring headaches if a wire does not have to be regarded as a transmission line. If the latter, luck can turn at any time with slight variations in components. This often explains why one or two units work in the lab, but a small manufacturing run has a high percentage of failures.

Parallel termination has the unfortunate consequence of heavily loading a driver because it is, after all, a small resistance connected directly across the signal and return paths. The driver sees a load of Z_O when it begins to switch its output but, once the line has stabilized, it still sees a load of R = Z_O. This is a substantial load with a 50- or 75-Ω transmission line. A 3.3-V driver would have to drive 66 mA into a 50-Ω load. If many bus signals need to be terminated, the power dissipation and stress on the driver ICs quickly mounts. This situation gets worse when terminating both ends of a bidirectional line.

There are several variants of parallel termination that seek to minimize the DC current drawn by the termination resistors. *Thevenin*, or *split termination,* operates using two resistors, each of which is chosen to be twice Z_O as shown in Fig. 18.8. One resistor terminates to ground and the other to the positive voltage rail. From an AC perspective, the positive voltage rail acts as a ground, and the parallel resistor combination appears as a single resistor equivalent of Z_O connected to ground. The benefit of split termination is that the maximum DC current drawn from the driver is halved, because a 100-Ω load is observed to the opposing voltage rail. When the driver drives to V_{DD}, the 100-Ω resistor to ground is the only load with a DC voltage drop across it. Split termination's disadvantage is that it always dissipates power, because the resistors establish a DC path between V_{DD} and ground.

The Thevenin concept can be carried further by employing a dedicated termination voltage rail, V_{TT}, that equals $V_{DD} \div 2$ and terminating to this rail using a resistor equal to Z_O as shown in Fig. 18.9. This scheme provides equivalent termination with less power dissipation, because the maximum voltage drop is $V_{DD} \div 2$ instead of V_{DD}. An additional benefit is that the terminator only dissipates power when the line is active. Bidirectional buses that are released to high-impedance states during idle will not load the termination resistor during that idle time.

Another variant of parallel termination uses a capacitor in series with the resistor to reduce power dissipation and is shown in Fig. 18.10. *AC termination* is suitable for clock signals or other DC balanced signals (e.g., 8B10B encoded signals), because such signals allow the capacitor to charge to $V_{DD} \div 2$ with the resultant benefits of reduced power dissipation as seen with $V_{DD} \div 2$ termination. Unbalanced signals remain at a static voltage for too long and charge the capacitor to either voltage rail. When a transition finally occurs, the full V_{DD} voltage drop appears across the terminator in a conceptually identical arrangement to basic parallel termination. The capacitor value must be chosen so that it maintains a nearly constant voltage during the balanced signal's period. A common 0.1-μF

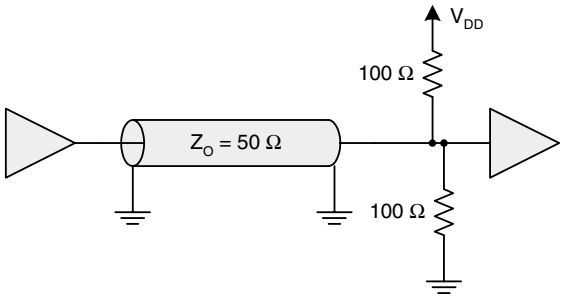

FIGURE 18.8 Thevenin termination.